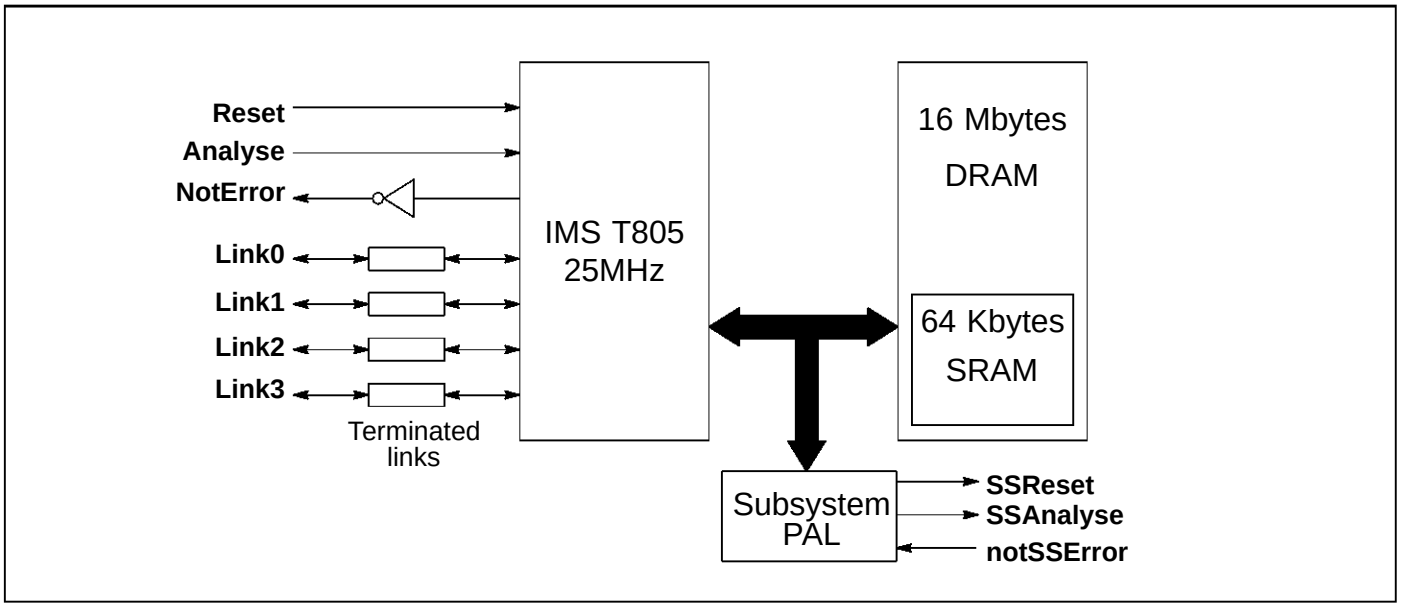
SGS-THOMSON MICROELECTRONICS

IMS B433

Size 4 16Mbyte HTRAM



FEATURES

- IMS T805 25 MHz Transputer
- 64 Kbytes of zero wait–state SRAM
- 16 Mbytes of single wait–state DRAM
- Subsystem controller circuitry
- Communicates via 4 INMOS serial links (Selectable between 10 or 20 Mbits/s)
- Package has only 16 active pins
- Designed to a published specification (*INMOS Technical Note 29*).

DESCRIPTION

The IMS B433 uses the IMS T805 25MHz transputer. The 16 Mbytes of single wait–state DRAM is sufficient to run large applications. Also provided is 64 Kbytes of fast SRAM (3 cycle), so any technique which puts most frequently accessed memory locations near the bottom of memory will speed up the processing.

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1.1 IMS B433 TRAM engineering data

1.1.1 Introduction

The IMS B433 is one of a range of INMOS **TRA**nsputer **M**odules (TRAMs) incorporating an IMS T805 transputer, 64 Kbytes of static RAM and 16 Mbytes of dynamic RAM. In effect, these TRAMs are board level transputers with a simple, standardized interface. They integrate processor, memory and peripheral functions allowing powerful, flexible, transputer based systems to be produced with the minimum of design effort.

Further details of the TRAM/motherboard philosophy and the full electrical and mechanical specification of TRAMs can be found in technical notes *Module Motherboard Architecture* and *Dual-In-Line Transputer Modules (TRAMs).* These are included in *The Transputer Development and i***q** *systems Databook* (INMOS document number 72 TRN 219 01).

If the user intends to design a custom motherboard, then *The Transputer Databook* (72 TRN 203 02) will also be required. These databooks are available as separate publications from INMOS.

1.1.2 Pin descriptions

Pin	In/Out	Function	Pin No.
System Services			
VCC, GND		Power supply and return	3,14
ClockIn	in	5MHz clock signal	8
Reset	in	Transputer reset	10
Analyse	in	Transputer error analysis	9
notError	out	Transputer error indicator (inverted)	11
Links			
LinkIn0-3	in	INMOS serial link inputs to transputer	13,5,2,16
LinkOut0-3	out	INMOS serial link outputs from transputer	12,4,1,15
LinkspeedA,B	in	Transputer link speed selection	6,7
Subsystem Services			
SubSystemReset	out	Subsystem reset	1b
SubSystemAnalyse	out	Subsystem error analysis	1c
notSubSystemError	in	Subsystem error indicator	1a

Table 1.1 IMS B433 Pin designations

Notes:

1 Signal names are prefixed by **not** if they are active low; otherwise they are active high.

2 Details of the physical pin locations can be found in Figure 1.3.

1.1.3 Standard TRAM signals

A TRAM can be regarded as a transputer with extra RAM attached, but with only 16 signals brought out to the TRAM pins. The majority of the TRAM pins function in exactly the same way as the corresponding transputer signals, which are detailed in *The Transputer Databook*. However, a few of these signals are slightly different from the transputer specification as follows:

1.2 notError (pin 11)

This is an open collector signal. It is driven low when there is an error; otherwise it is pulled high by a resistor on the motherboard. This enables the **notError** outputs on several TRAMs to be wire-ORed together. (The TRAM specification recommends that no more than 10 **notError** outputs are connected together).

1.3 LinkSpeedA and LinkSpeedB (pins 6 and 7)

LinkSpeedA and **LinkSpeedB** set the speed of transputer link 0 and links 1-3 respectively. When the appropriate input is low, the link(s) operate at 10 Mbits/s, and when high the link(s) operate at 20 Mbits/s.

1.4 Link signals

Whilst the links obey a protocol identical to that described in *The Transputer Databook*, there are some differences in the electrical characteristics.

1.4.1 LinkIn0–3

The link inputs have pull-down resistors to ensure that they are disabled when they are not connected. Diodes are also included for protection against electrostatic discharge.

1.4.2 LinkOut0–3

The link outputs have resistors connected in series for matching to a 100 ohm transmission line.

1.5 Subsystem signals

The IMS B433 has a subsystem port in addition to the usual TRAM signals. This enables the TRAM to reset or analyse a subsystem of other TRAMs and/or motherboards. The polarity of these signals is the same as that of the **Reset**, **Analyse** and **notError** standard TRAM signals. Therefore, the IMS B433 subsystem can drive other TRAMs on the same motherboard with no intermediate logic. However, **SubSystemReset** and **SubSystemAnalyse** must go through inverting buffers if they are to drive a subsystem off the motherboard.

These subsystem signals are accessed by writing or reading to control registers in the transputer memory space.

1.6 Memory configuration

The IMS B433 is able to access 16 Mbytes of memory. This is comprised of 4 Kbytes of internal transputer memory, 60 Kbytes of external SRAM and 16320 Kbytes of external DRAM. There are, in fact, 64 Kbytes of SRAM components and16 Mbytes of DRAM components on the board, but the address spaces of each type of memory are superimposed. Therefore, the total memory available is limited to 16 Mbytes.

1.6.1 Location of external memory

Tables 1.2 and 1.3 show the start addresses of the different types of external memory on the IMS B433 (the ‘‘#’’ sign indicates a hexadecimal number). The internal RAM on the IMS T805 occupies the first 4 Kbytes of address space.

	Hardware byte address
From:	#80001000
To:	#8000FFFF

Table 1.2 Location of external SRAM on the IMS B433

	Hardware byte address
From:	#80010000
To:	#80FFFFFF

Table 1.3 Location of external DRAM on the IMS B433

Since the internal memory on the IMS T805 is 1 cycle, the external SRAM is 3 cycle and the DRAM is 4 cycle, a memory speed hierachy is established. This architecture allows programmers to structure their code for optimum performance.

1.6.2 Subsystem register locations

The subsystem register addresses start at hardware address #00000000 in all TRAMs that utilize a 32-bit processor, allowing software compatibility between TRAMs. These registers are located as shown in Table 1.4.

Register	Hardware byte address
SubSystemReset (write only)	#00000000
SubSystemAnalyse (write only)	#00000004
notSubSystemError (read only)	#00000000

Table 1.4 Subsystem address locations

Setting bit 0 in either the reset or the analyse registers asserts the corresponding signal. Similarly, clearing bit 0 deasserts the signal. When an error occurs in the subsystem, bit 0 of the error location becomes set.

Byte locations #00000008 and #0000000C are unused. The subsystem registers are repeated at every sixteenth byte location in the positive address space. See Figure 1.1.

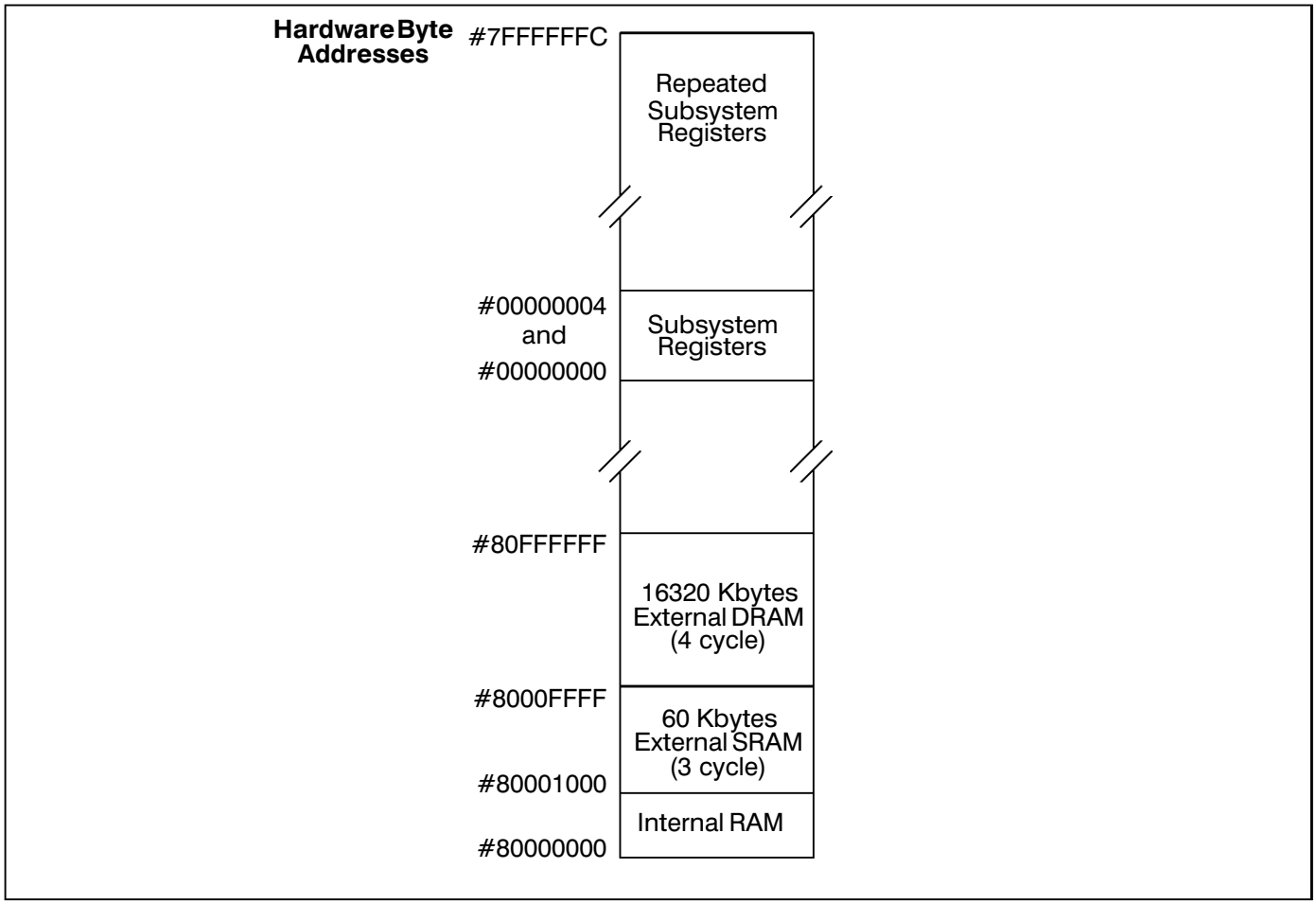

Figure 1.1 Memory map

1.7 Mechanical details

Figure 1.2 indicates the vertical dimensions of a single IMS B433 and Figure 1.3 shows the outline drawing of the IMS B433.

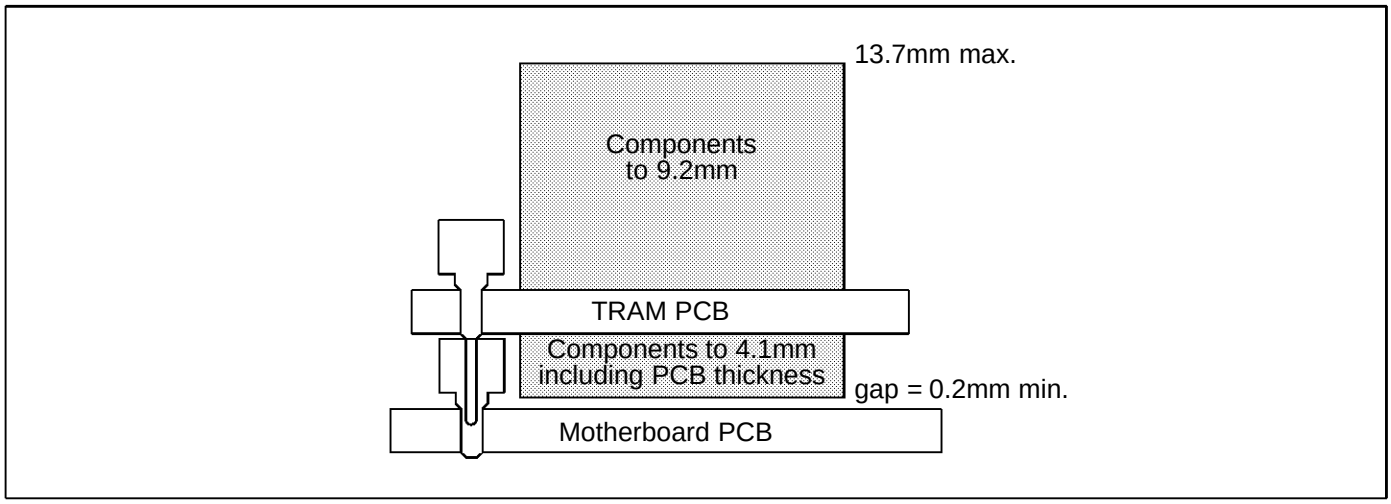

Figure 1.2 IMS B433 height specification

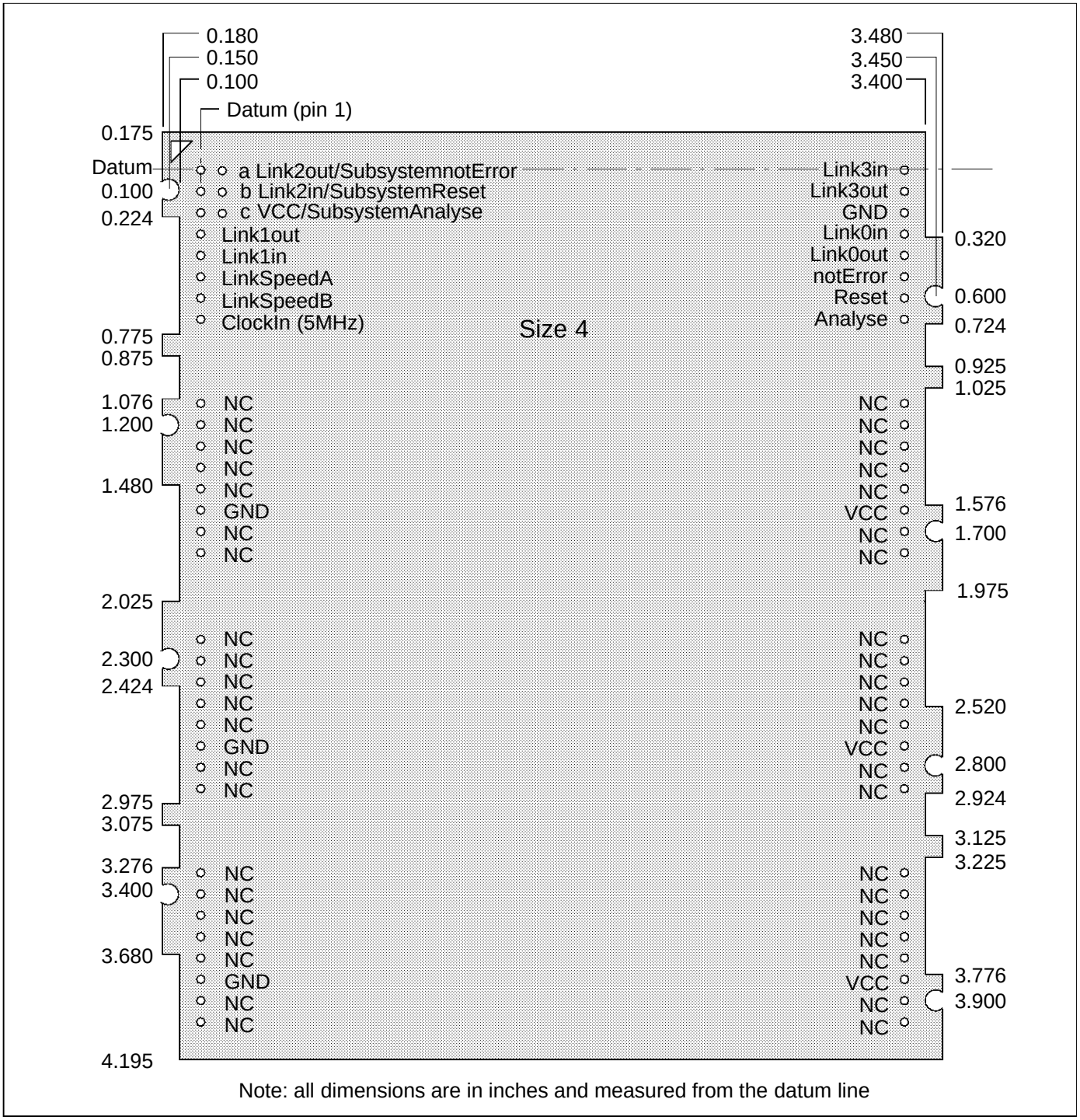

Figure 1.3 IMS B433 outline drawing

1.8 Installation

Since the IMS B433 contains CMOS components, all normal precautions to prevent static damage should be taken.

The IMS B433 is supplied with spacer pin strips attached to the TRAM pins on the underside of the board. These spacers perform two functions. Firstly, they help to protect the TRAM pins during transit. Secondly, they can be used to space the TRAMs off the motherboard. If there are no components mounted on the motherboard TRAM slot, then the spacer strips should be removed before the TRAM is inserted.

If the subsystem signals are required, plug a 3-way header strip into the solder-side sockets (aside pins 1-3) on the IMS B433.

Plug the IMS B433 into the motherboard. Where the IMS B433 is being used with an INMOS motherboard, the silk screened triangle marking pin 1 on the IMS B433 (see Figure 1.3) should be aligned with the silk screened triangle that appears in the corner of the appropriate TRAM slot.

Should it be necessary to unplug the IMS B433, it is advised that it is gently levered out while keeping it as flat as possible. As soon as the IMS B433 is removed, the spacer pin strips should be refitted to the TRAM to protect the pins.

1.9 Specification

TRAM feature	IMS B433-16	Unit	Notes
Transputer type	IMS T805-25		
Number of transputers	1		
Number of INMOS serial links	4		
Amount of SRAM	64	Kbyte	
SRAM ‘‘wait states’’	0		
SRAM cycle time	120	ns	
Amount of DRAM	16	Mbyte	
DRAM ‘‘wait states’’	1		
DRAM cycle time	160	ns	
Subsystem controller	Yes		
Peripheral circuitry	None		
Parity	No		
Size (TRAM size)	4		
Length	3.66	inch	
Pitch between pins	3.30	inch	
Width	4.35	inch	
Component height above PCB	9.2	mm	
Component height below PCB	3.7	mm	1
Weight	110	g	
Storage temperature	0–70	^{o}C	
Operating temperature	0–50	^{o}C	2
Power supply voltage (VCC)	4.75–5.25	Volt	
Power consumption	7	W	3

Table 1.5 IMS B433 specification

Notes:

1 This dimension includes the thickness of the PCB.

2 The figure quoted refers to the ambient air temperature.

3 The power consumption is the worst case value obtained when a sample of IMS B433 TRAMs were tested (running a program that utilised all four links and accessed memory simultaneously) at a supply voltage (VCC) of 5.25 V.

1.10 Ordering Information

Description	Order Number
IMS B433 TRAM with IMS T805-25	IMS B433-16

Table 1.6 Ordering information